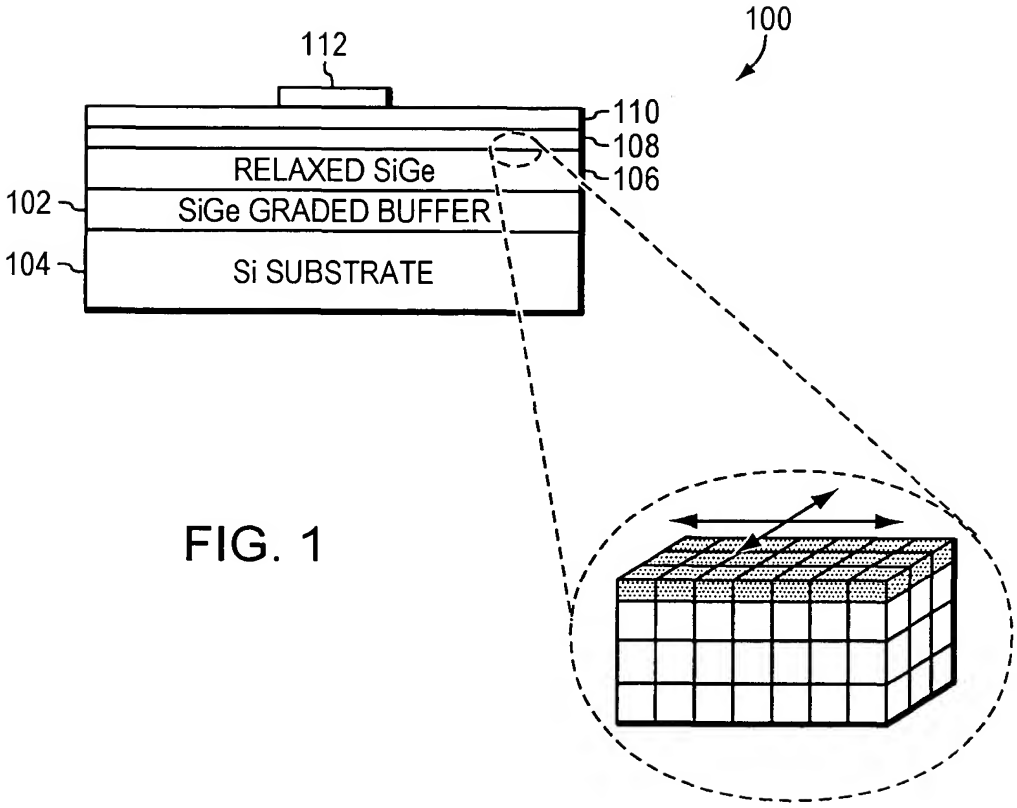
100
112
110
108
106
RELAXED SiGe
102
SiGe GRADED BUFFER
104
Si SUBSTRATE

FIG. 1

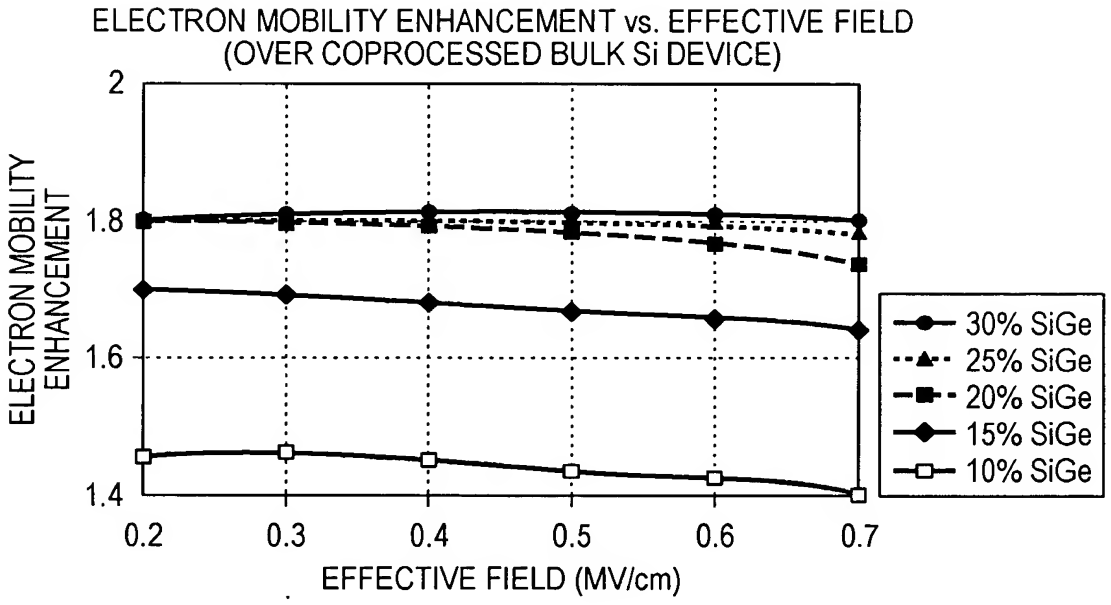
ELECTRON MOBILITY ENHANCEMENT vs. EFFECTIVE FIELD
(OVER COPROCESSED BULK Si DEVICE)
ELECTRON MOBILITY ENHANCEMENT
2
1.8
1.6
1.4
0.2
0.3
0.4
0.5
0.6
0.7
EFFECTIVE FIELD (MV/cm)
30% SiGe
25% SiGe
20% SiGe
15% SiGe
10% SiGe

FIG. 2A

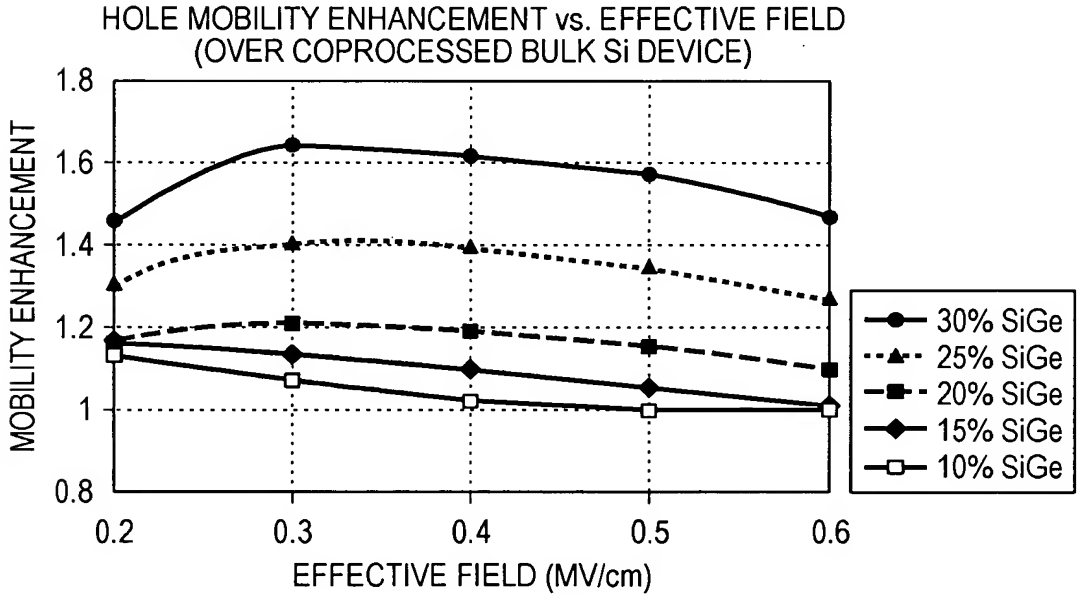
HOLE MOBILITY ENHANCEMENT vs. EFFECTIVE FIELD
(OVER COPROCESSED BULK Si DEVICE)
MOBILITY ENHANCEMENT
1.8
1.6
1.4
1.2
1
0.8
0.2
0.3
0.4
0.5
0.6
EFFECTIVE FIELD (MV/cm)
30% SiGe
25% SiGe
20% SiGe
15% SiGe
10% SiGe

FIG. 2B

TYPE OF SURFACE	AVERAGE ROUGHNESS (nm)
AS-GROWN GRADED COMPOSITION RELAXED SiGe	7.9
PLANARIZED SiGe	0.57
REGROWTH SiGe	-0.6

FIG. 3

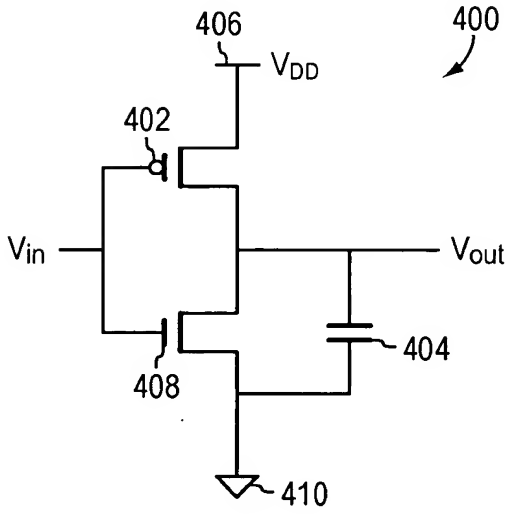

FIG. 4

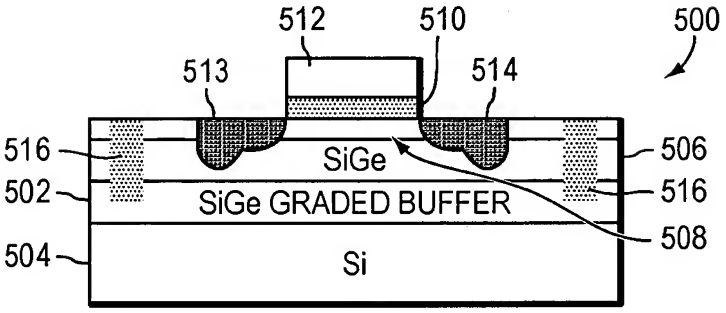
512
510
500
513
514
516
SiGe
506
502
SiGe GRADED BUFFER
516
508
504
Si

FIG. 5A

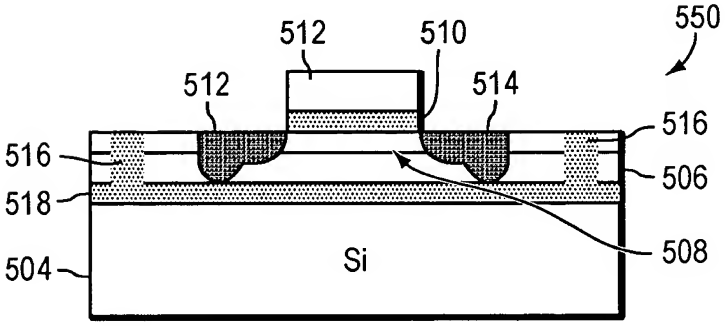
512
510
550
512
514
516
516
506
518
508
504
Si

FIG. 5B

	n ENHANCEMENT	p ENHANCEMENT
$Si_{0.8}Ge_{0.2}$	1.75	1
$Si_{0.7}Ge_{0.3}$	1.8	1.4

FIG. 6

	BULK SILICON	STRAINED-Si ON 20% SiGe: HIGH SPEED	STRAINED-Si ON 30% SiGe: HIGH SPEED	STRAINED-Si ON 20% SiGe: LOW POWER	STRAINED-Si ON 30% SiGe: LOW POWER
n ENHANCEMENT	1	1.75	1.8	1.75	1.8
p ENHANCEMENT	1	1	1.4	1	1.4
W_p (μm)	5.4	5.4	5.4	5.4	5.4
W_n (μm)	1.8	1.8	1.8	1.8	1.8
L_n, L_p (μm)	1.2	1.2	1.2	1.2	1.2
C_L (fF)	32	32	32	32	32
V_{DD} (V)	5	4.7	4.4	4.3	3.8
NM_H (V)	2.053	2.218	1.949	2.037	1.682
NM_L (V)	2.067	1.654	1.721	1.542	1.504
t_{pHL} (psec)	211.3	133.7	141.6	152.2	180.1
t_{pLH} (psec)	195.8	220.0	173.3	254.8	226.9
t_p (psec)	203.5	176.9	157.4	203.5	203.5
POWER (mW)	3.93	3.93	3.93	2.87	2.21
% SPEED INCREASE	-	15.1%	29.3%	-	-
% POWER REDUCTION	-	-	-	27.0%	43.7%

FIG. 7

	BULK SILICON	STRAINED-Si ON 20% SiGe: CONSTANT V_{DD}	STRAINED-Si ON 30% SiGe: CONSTANT V_{DD}	STRAINED-Si ON 20% SiGe: HIGH SPEED SYMMETRICAL INVERTER	STRAINED-Si ON 30% SiGe: HIGH SPEED SYMMETRICAL INVERTER	STRAINED-Si ON 20% SiGe: LOW POWER SYMMETRICAL INVERTER	STRAINED-Si ON 30% SiGe: LOW POWER SYMMETRICAL INVERTER
n ENHANCEMENT	1	1.75	1.8	1.75	1.8	1.75	1.8
p ENHANCEMENT	1	1	1.4	1	1.4	1	1.4
W_p (μm)	5.4	5.4	5.4	9.45	6.94	9.45	6.94
W_n (μm)	1.8	1.8	1.8	1.8	1.8	1.8	1.8
L_n, L_p (μm)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
C_L (fF)	32	32	32	32	32	32	32
V_{DD} (V)	5	5	5	4.3	4.2	3.5	3.5
NM_H (V)	2.053	2.376	2.198	1.782	1.770	1.5018	1.4796
NM_L (V)	2.067	1.751	1.923	1.794	1.781	1.5101	1.4876
t_{pHL} (psec)	211.3	120.7	117.4	152.0	149.5	204.4	204.1
t_{pLH} (psec)	195.8	195.8	139.9	145.4	143.3	202.6	202.9
t_p (psec)	203.5	158.3	128.6	148.7	146.4	203.5	203.5
POWER (mW)	3.93	5.06	6.22	3.93	3.93	1.95	1.89
% SPEED INCREASE	-	28.6%	58.3%	36.9%	39.0%	-	-
% POWER REDUCTION	-	-	-	-	-	50.4%	52.0%

FIG. 8

Title: METHOD OF FABRICATING CMOS INVERTER AND INTEGRATED CIRCUITS UTILIZING STRAINED SILICON SURFACE CHANNEL MOSFETS
Inventors: Eugene A. Fitzgerald et al.
Serial No. *Not yet assigned*
Atty Docket No. ASC-044C1
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV192309385US

	BULK SILICON	STRAINED-Si ON 20% SiGe: HIGH SPEED	STRAINED-Si ON 30% SiGe: HIGH SPEED	STRAINED-Si ON 20% SiGe: LOW POWER	STRAINED-Si ON 30% SiGe: LOW POWER
n ENHANCEMENT	1	1.75	1.8	1.75	1.8
p ENHANCEMENT	1	1	1.4	1	1.4
W_p (μm) -	3.11	4.12	3.53	4.12	3.53
W_n (μm)	1.8	1.8	1.8	1.8	1.8
L_n, L_p (μm)	1.2	1.2	1.2	1.2	1.2
C_L (fF)	22.5	26.7	24.2	26.7	24.2
V_{DD} (V)	5	4.5	4.3	4.4	3.8
NM_H (V)	2.370	2.275	2.123	2.220	1.872
NM_L (V)	1.756	1.485	1.511	1.458	1.371
t_{pHL} (psec)	148.4	117.3	109.3	121.5	132.4
t_{pLH} (psec)	238.5	254.8	204.9	265.3	254.4
t_p (psec)	193.4	186.0	157.1	193.4	193.4
POWER (mW)	2.90	2.90	2.90	2.66	1.83
% SPEED INCREASE	-	4.0%	23.1%	-	-
% POWER REDUCTION	-	-	-	8.4%	37.1%

FIG. 9

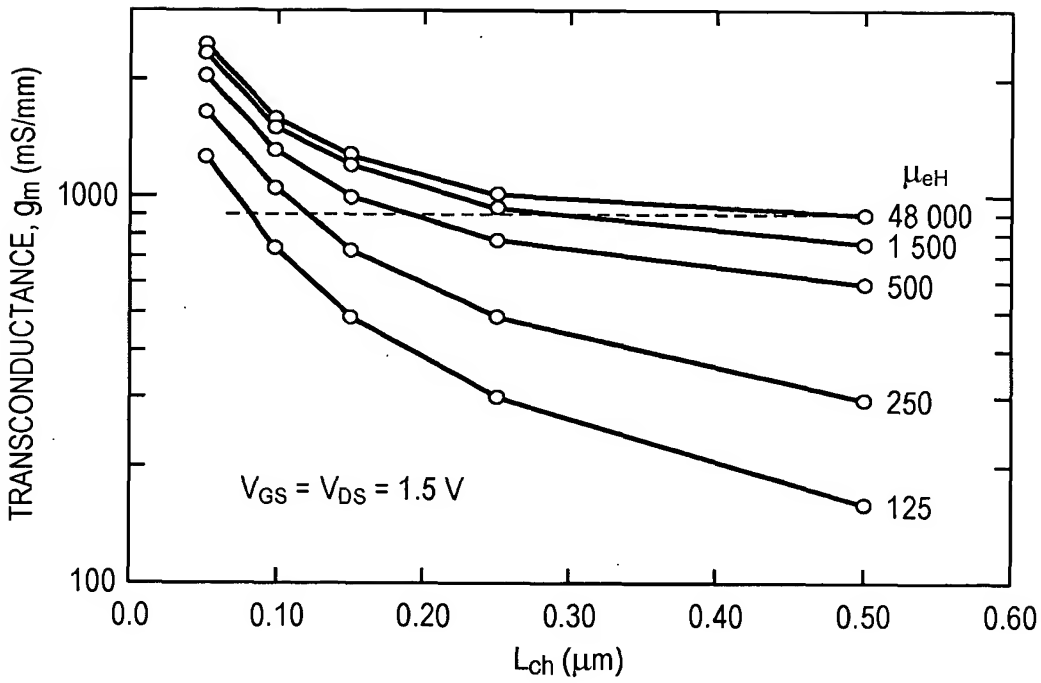
TRANSCONDUCTANCE, g_m (mS/mm)
1000
100
0.0
0.10
0.20
0.30
0.40
0.50
0.60
L_{ch} (μm)
μ_{eH}
48 000
1 500
500
250
125
$V_{GS} = V_{DS} = 1.5$ V

FIG. 10

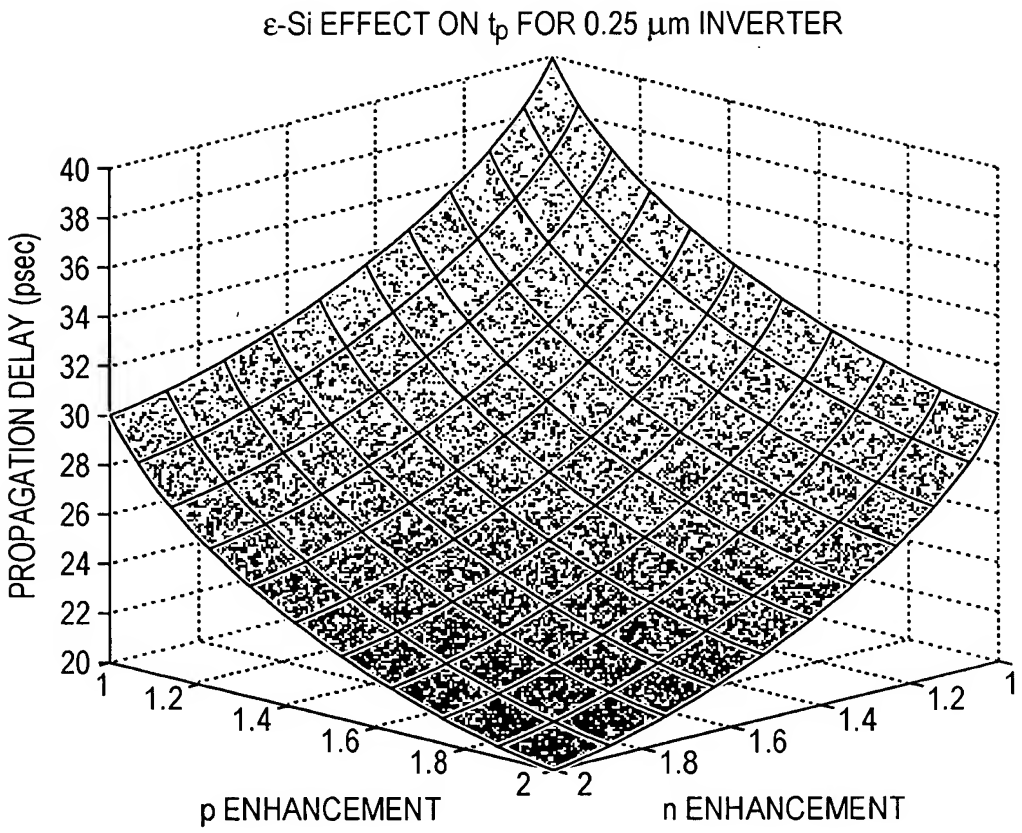
ε-Si EFFECT ON t_p FOR 0.25 μm INVERTER
PROPAGATION DELAY (psec)
40
38
36
34
32
30
28
26
24
22
20
1
1.2
1.4
1.6
1.8
2
p ENHANCEMENT
n ENHANCEMENT

FIG. 11

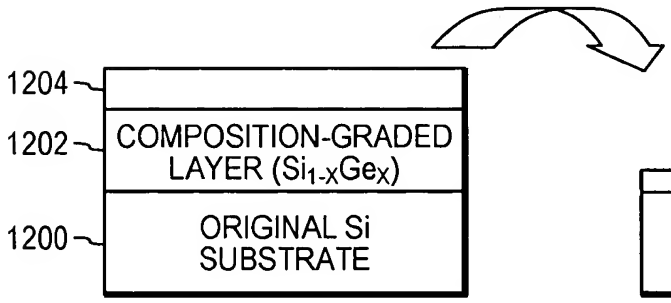

FIG. 12A

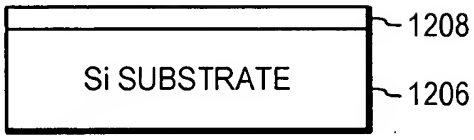

FIG. 12B

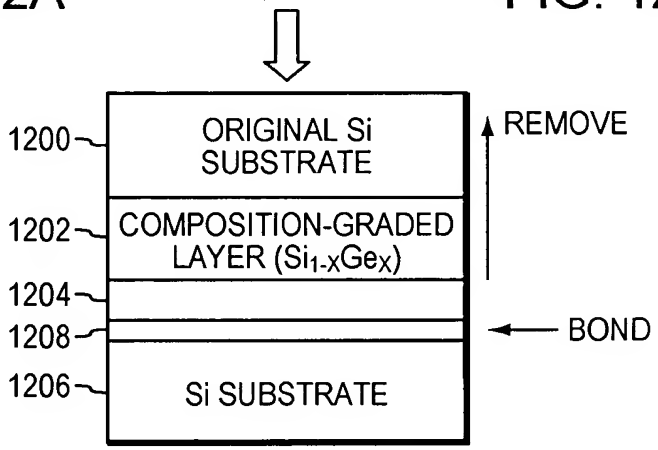

FIG. 12C

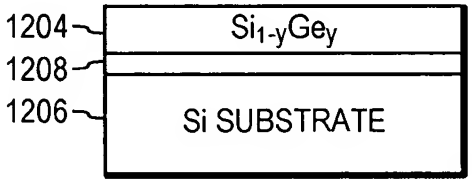

FIG. 12D

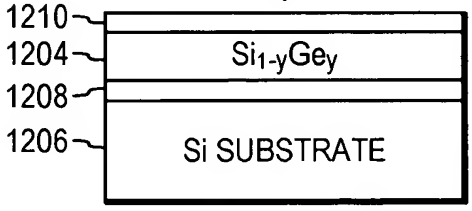

FIG. 12E

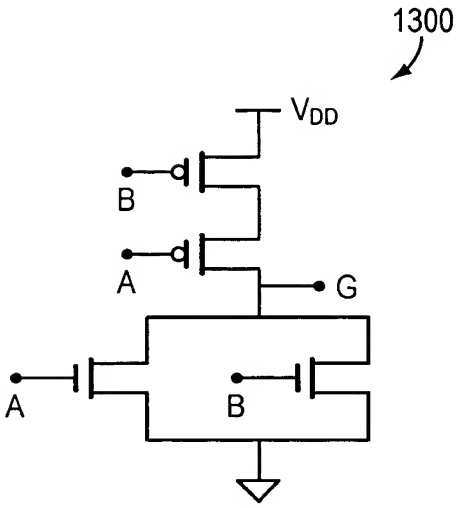

FIG. 13A

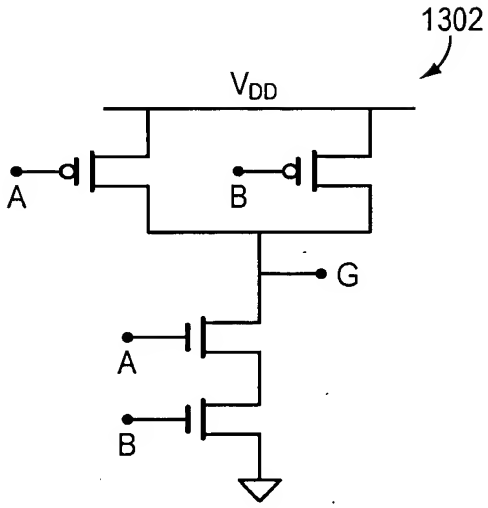

FIG. 13B

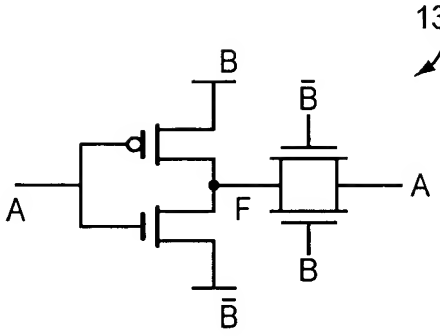

FIG. 13C